

# Low-Resistance Titanium Contacts and Thermally Unstable Nickel Germanide Contacts on p-Type Germanium

Hao Yu, *Student Member, IEEE*, Marc Schaeckers, Tom Schram, Wolfgang Aderhold, Abhilash J. Mayur, Jerome Mitard, Liesbeth Witters, Kathy Barla, Nadine Collaert, Naoto Horiguchi, Aaron Voon-Yew Thean, and Kristin De Meyer, *Fellow, IEEE*

**Abstract**—Ti/p-Ge and NiGe/p-Ge contacts are compared on both planar- and fin-based devices. Ti/p-Ge contacts show low contact resistance, while NiGe/p-Ge devices show short circuit problems due to thermally driven Ni diffusion. Considering the thermal budget in the standard backend of line processing for CMOS, Ti is more suitable for p-Ge devices. A low Ti/p-Ge contact resistivity of  $1.1 \times 10^{-8} \Omega \cdot \text{cm}^2$  is achieved by using a multi-pulse laser annealing technique for B activation.

**Index Terms**—Contact resistance, contact resistivity, p-type germanium, transmission line model, germanide.

## I. INTRODUCTION

WITH its superior hole mobility, p-type Ge is an attractive channel material for p-MOSFETs. The small-dimension p-Ge FinFETs have successfully been integrated onto 300 mm Si wafers [1], [2]. With shrinking contact sizes in modern transistors, metal/semiconductor contact resistivities ( $\rho_c$ ) have become increasingly critical. However, only a few  $\rho_c$  studies have been reported on p<sup>+</sup>-Ge [3]–[9], which usually use p<sup>+</sup>/n Ge junctions deeper than 100 nm and thus cannot be directly compared to downscaled devices. Therefore, device-oriented investigations on the p-Ge contacts are required.

In this work, we compare NiGe contacts and Ti contacts on both planar and nanoscale 3D structures with shallow p<sup>+</sup>-Ge junctions. We find that NiGe contacts degrade seriously due to the thermal budget in standard processing, while Ti contacts show low  $\rho_c$  and adequate stability. Ti is thus a better contact candidate for p-Ge. Low  $\rho_c$  of  $1.1 \times 10^{-8} \Omega \cdot \text{cm}^2$  is achieved by Ti/p-Ge with a multi-pulse laser dopant activation technique.

## II. EXPERIMENTS

With generally low Schottky barriers [12], [13], the contacts on p<sup>+</sup>-Ge usually have  $\rho_c$  near or below  $1 \times 10^{-6} \Omega \cdot \text{cm}^2$  [3]–[9]. These low  $\rho_c$  challenge the accuracy

of traditional  $\rho_c$  test structure. Recently,  $\rho_c$  test models with high accuracy have been developed [14]–[20]. In this work, we applied circular transmission line model (CTLM) with refined  $\rho_c$  extraction procedures [18], and nanoscale transmission line model on fin-like structures (Fin-TLM) [19].

The CTLM structures were fabricated on 300 mm Si wafers. 600 nm thick epitaxial Ge was grown. A phosphorus well was formed by implantation and annealing. A 5 keV  $1 \times 10^{15} \text{ cm}^{-2}$  Ge preamorphization implantation (PAI) was performed, followed by a 1.6 keV  $1 \times 10^{15} \text{ cm}^{-2}$  B ion implantation (I/I). B was activated with either a 600°C 5 min rapid thermal process (RTP) in N<sub>2</sub> or a laser anneal. The laser anneal was performed by a Laser Thermal Processing tool from Applied Materials, which provides a controlled laser energy fluence with a pulse width of tens of ns [21]. Single-pulse laser (SPL) or multi-pulse laser (MPL) was applied, and the p<sup>+</sup>-Ge region was melt and recrystallized [21]. Details of the rest of the CTLM patterning process can be found elsewhere [18], [20]. For Ti/p-Ge samples, 5 nm PVD Ti was deposited on p-Ge. For NiGe/p-Ge samples, 10 nm PVD Ni was deposited; and NiGe was formed by a 290°C 30s RTP, a selective wet etch, and a 355°C 30s RTP [11].

The Fin-TLM fabrication started with Ge epitaxy in 100 nm wide Si STI trenches. A phosphorus well was formed. The Ge PAI, B I/I, RTP activation, and the contact metal formation processes were identical to those used for CTLM. Then the Fin-TLMs were interconnected with CVD W and received a 20 min 400°C H<sub>2</sub> passivation sintering. W CVD (at 425°C) and H<sub>2</sub> sintering compose a thermal budget comparable to that in typical FinFET processing [1]. Eventually, a wafer-backside Al was deposited to enable p<sup>+</sup>/n Ge diode measurement.

Schematics of CTLM and Fin-TLM are shown in Fig. 1. The CTLM structures have an inner radius  $r_0$  of 50  $\mu\text{m}$  and electrode spacing of 0.35–10  $\mu\text{m}$ ; the Fin-TLM structures have width of 100 nm and electrode spacing of 0.11–9.01  $\mu\text{m}$ . In Fig. 1e, parasitic factors, the metal resistance and the substrate leakage, are illustrated in TLM, which may cause inaccurate  $\rho_c$  extraction. The metal impact was suppressed using the method in [18]. To eliminate the substrate leakage, a n-Ge well with P concentration of  $\sim 4 \times 10^{17} \text{ cm}^{-3}$  was formed beneath p<sup>+</sup>-Ge. As shown in Fig. 1f, the p<sup>+</sup>/n junction creates a  $\sim 0.5$  eV high ( $V_d$ ) and  $\sim 50$  nm thick ( $W_d$ ) potential barrier, which confines the TLM operating current within p<sup>+</sup>-Ge. Also, low bias voltage ( $\leq \pm 0.1\text{V}$ ) was used in the TLM measurement, and TLM with relatively small spacing ( $\leq 10 \mu\text{m}$ ) were adopted in the fitting, which suppress

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H. Yu and K. De Meyer are with the Department of Electrical Engineering, Katholieke Universiteit, Leuven 3001, Belgium, and also with imec, Leuven 3001, Belgium (e-mail: hao.yu@imec.be).

M. Schaeckers, T. Schram, J. Mitard, L. Witters, K. Barla, N. Collaert, N. Horiguchi, and A. Voon-Yew Thean are with imec, Leuven 3001, Belgium.

W. Aderhold and A. J. Mayur are with Applied Materials, Sunnyvale, CA 84085 USA.

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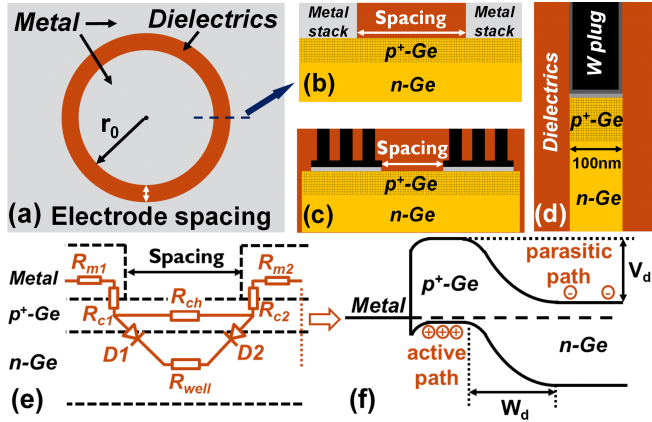


Fig. 1. Schematics of a) top-view and b) section-view of CTLM; and cross-section views of Fin-TLM from the section c) through or d) across the fins. e) An equivalent circuit of TLM model in section-view. f) Energy band diagram across metal/ $p^+$ -Ge/ $n$ -Ge stack.

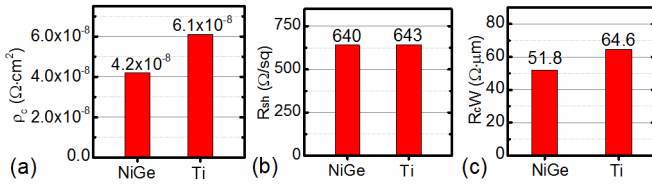


Fig. 2. a)  $\rho_c$ , b)  $R_{sh}$  and c)  $R_c$  of NiGe/ $p$ -Ge and Ti/ $p$ -Ge, extracted using CTLM.

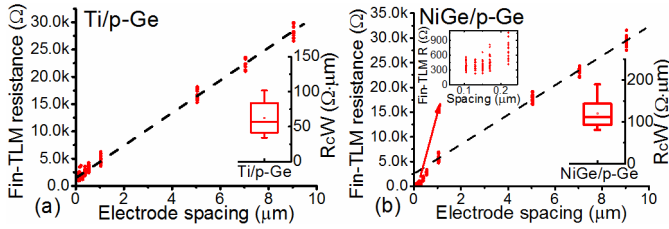


Fig. 3. a) Ti/ $p$ -Ge and b) NiGe/ $p$ -Ge Fin-TLM resistance-spacing data. 20 sets of data were measured for each condition. The dashed lines illustrate the data fitting (for NiGe, the data with narrow spacing are excluded in the fitting). The extracted  $R_c$  are shown in the insets to the right of a) and b).

the leakage current through D1 and D2 in Fig. 1e. Samples were measured with HP4156c parameter analyzer.

### III. TITANIUM OR NiGe FOR $p$ -Ge?

Ti/ $p$ -Ge and NiGe/ $p$ -Ge are first compared on CTLM in Fig. 2. Despite the large work function difference between Ti ( $\sim 4.3\text{eV}$ ) and NiGe ( $\sim 5.2\text{eV}$ ), their  $\rho_c$  on  $p^+$ -Ge are close. This is because of the strong Fermi level pinning at the Ge surface [12], [13] which reduces the sensitivity of  $\rho_c$  to the metal work function. Contact resistances ( $R_c$ ) are also compared. When the electrode length is much larger than the transfer length ( $L_t$ )— $L_t$  is  $\sim 100$  nm in this work, the  $R_c$  and  $\rho_c$  are correlated by [22]

$$R_c W = \sqrt{\rho_c R_{sh}} \quad (1)$$

where  $W$  is the width of the contact, and  $R_{sh}$  is the sheet resistance of the  $p^+$ -Ge.

Next, Ti and NiGe contacts are compared on Fin-TLM in Fig. 3.  $R_c W$  of Ti/ $p$ -Ge from Fin-TLM is close to that from CTLM. However, NiGe contacts show problems: 1) contrary to the CTLM results,  $R_c W$  of NiGe is higher than that of Ti; 2) the resistances of the NiGe Fin-TLMs with small spacing

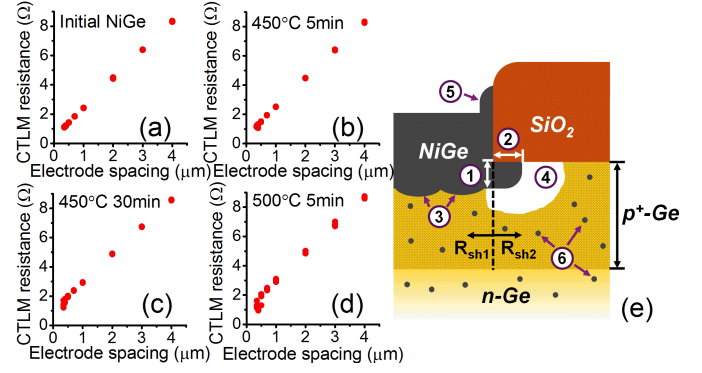


Fig. 4. CTLM resistance-spacing data of a) initial NiGe/ $p$ -Ge samples, and those annealed with b) 450°C 5 min, c) 450°C 30 min, or d) 500°C 5 min RTP. Four sets of data were measured for each condition. Schematic of NiGe related problems in TLM are illustrated in e).

fall out of the linear resistance-spacing trend. We speculate that short circuits occurred in those small-spacing TLMs due to Ni diffusion [23]. Recently, an enormous leakage induced by Ni diffusion was observed from the shallow  $n^+/p$  Ge junction [24].

As shown in Fig. 4a, the short circuit is not seen on the as formed NiGe/ $p$ -Ge CTLM samples. We consider that, besides the structure difference, another major difference between Fin-TLM and CTLM is the thermal budget in the post-contact process: Fin-TLM saw two W CVD steps at  $\sim 425^\circ\text{C}$  and a  $\text{H}_2$  sintering step at  $400^\circ\text{C}$  for 20 min; CTLM was free of the above steps, and the highest process temperature was at  $\sim 370^\circ\text{C}$ . To find out if it is the heating process that causes the short circuit, RTP in  $\text{N}_2$  was performed on the NiGe CTLM samples. In Fig. 4b, signs of degradation show up after a 450°C 5 min RTP: the small-spacing CTLMs become randomly shorted. An increased RTP time (Fig. 4c) or RTP temperature (Fig. 4d) aggravates the degradation. Now we conclude that the short circuit is a thermally driven problem.

In Fig. 4e, the potential NiGe related problems are illustrated: 1) vertical growth of NiGe and consumption of Ge, 2) lateral growth of NiGe, 3) NiGe agglomeration [10], 4) void formation [11], 5) NiGe overgrowth [11], and 6) Ni diffusion [23]. Some of these problems cause inaccurate TLM fitting and  $\rho_c$  extraction for NiGe contacts, while some create potential stability problems for NiGe based devices. Thin Ni, well controlled germanidation process, and low post-germanidation thermal budget are required to suppress these problems [11]. Note that Problem 1-5 would affect TLMs with all spacing, while only Problem 6, Ni diffusion, can lead to short circuit problems. Ni and Cu are two fastest diffusion impurities in Ge [23], which can diffuse from the contacts into the bulk during a heating process, precipitate at Ge lattice imperfections during cooling, and thereby form local defects, e.g. local germanide precipitates [23]. In small-spacing TLMs, two NiGe electrodes are closer to each other, and therefore there is a higher chance for those local defects merging into conductive paths. Therefore, considering the small channel length in modern CMOS devices and the thermal budget in standard process, NiGe and  $\text{Cu}_3\text{Ge}$  contacts do not apply to Ge devices, despite their reported low  $\rho_c$  on  $p$ -Ge [3], [5], [8], [9]. Note that if the shorted TLMs are included in the fitting, they cause underestimation of  $\rho_c$  and wrong conclusions of germanide contacts.

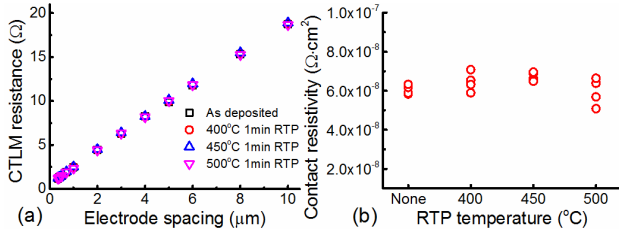


Fig. 5. Ti/p-Ge CTLM a) resistance-spacing data and b)  $\rho_c$  results with and without RTP post-metal annealing. Four sets of CTLM data were obtained for varying temperature. Data with and without RTP are overlapped in a), so only one set of data is shown for each case in a) for clarity.

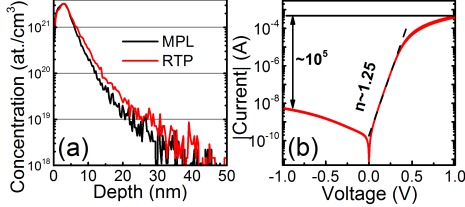


Fig. 6. a) B profile in the p<sup>+</sup>-Ge after MPL and RTP, measured with SIMS on CTLM. b) IV curves of five (overlapped) Ge p<sup>+</sup>/n diodes with RTP B activation and Ti contacts, measured by sweeping voltage between Fin-TLM electrodes and wafer chuck. The active area of p<sup>+</sup>/n junctions in b) is 100 nm × 10 μm.

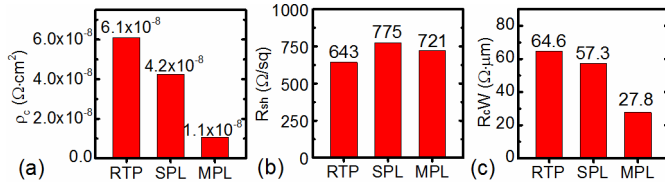


Fig. 7. a)  $\rho_c$ , b)  $R_{sh}$  and c)  $R_c$  of Ti/p<sup>+</sup>-Ge contacts extracted using CTLM.

Ni-Ge reaction starts at 250°C [25], and NiGe gets agglomerated at as low as 500°C [10]. In contrast, a Ti thin film remains unreacted on a Ge substrate until ~450°C [25]; from 450°C, Ti intermixes with Ge, and the first clear Ti-Ge alloy phase occurs at ~550°C [25]. In Fig. 5, the thermal stability of Ti/p-Ge contacts is verified with an RTP experiment on CTLM. In conclusion, Ti is a better metal candidate for p-Ge contacts because of its low  $\rho_c$  and its thermal stability with Ge. Moreover, Ti has an O scavenging ability, i.e. Ti can clean the oxide residues on a Ge surface. We found that 5nm Ti can remove ~1nm oxide layer and still provide decent  $\rho_c$ , because of the high O solubility and fast O diffusion in Ti [26]. The O removal can be simply triggered by the heat in device processing after Ti deposition (~400°C, several min) [26].

#### IV. MULTI-PULSE LASER (MPL) FOR B ACTIVATION

In this work, low-energy Ge PAI and B I/I were applied. The B profiles from both the RTP and MPL activated shallow p<sup>+</sup>/n Ge junctions are shown in Fig. 6a. The IV curves of five RTP activated p<sup>+</sup>/n Ge diodes are shown in Fig. 6b, which are characterized by an on/off ratio of ~10<sup>5</sup>, an ideality factor ( $n$ ) of 1.25, and high repeatability. (Unfortunately, ns laser activated p<sup>+</sup>/n Ge diodes are unavailable in this work.)

In Fig. 7, Ti/p-Ge contacts with different B activation methods are compared: in terms of  $\rho_c$ , RTP > SPL > MPL. As demonstrated in the field emission theory [27],

$$\rho_c \propto \exp\left(C \frac{\phi_b}{\sqrt{N_a}}\right) \quad (2)$$

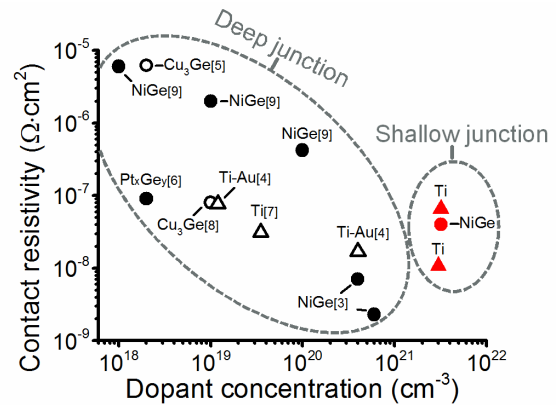


Fig. 8. Benchmark for  $\rho_c$  on p<sup>+</sup> Ge. Red symbols are from this work; black ones from literature. Circular symbols are germanide contacts; triangles are pure metal contacts. Hollow symbols are based on active dopant concentration; solid ones based on physical dopant concentration. “Deep junction” denotes studies using junctions deeper than 100 nm.

where  $C$  is a constant,  $\phi_b$  is the Schottky barrier height, and  $N_a$  is the active B concentration at p<sup>+</sup>-Ge surface. Considering the same  $\phi_b$  of Ti/p-Ge among all samples, the  $\rho_c$  results in Fig. 7a indicate that the highest  $N_a$  is achieved by the MPL.

As shown in Fig. 7b, the  $R_{sh}$  is high for all samples: low hole mobility could be inferred, which probably results from the low-energy PAI used in this work. In principle, PAI is beneficial for Ge p<sup>+</sup>/n shallow junction formation: it prevents the B channeling, adds the abruptness of the B profile and improves B activation [28], [29]. However, Chao *et al.* [28] also find that, when the depth of preamorphized Ge is less than the B projected range, the heat from B I/I leads to imperfect Ge recrystallization at the amorphous/crystalline Ge interface, thereby forming defects in the p<sup>+</sup>-Ge and degrading the hole mobility. Using SRIM simulation [30], we find that the amorphized Ge in this work is less than 15 nm in depth with the 5keV Ge I/I, which is shallower than the B profiles in Fig. 6a.

This problem with PAI leads to a dilemma: a low-energy PAI is insufficient and causes a high  $R_{sh}$ , but a high-energy PAI is incompatible with the small-dimension devices—perfect Ge recrystallization on fin structures is even more difficult. To form a shallow Ge p<sup>+</sup>/n junction with both low  $R_{sh}$  and high  $N_a$ , the insitu B doping during Ge epitaxy [9] is probably the most promising doping solution. The MPL introduced can serve as an auxiliary technique to further boost  $N_a$ . Compatibility of MPL with fin structures will be studied in the future.

To our knowledge, both shallow p<sup>+</sup>/n Ge junction formation [31] and the  $\rho_c$  on shallow p<sup>+</sup>/n Ge junction have rarely been studied. All of the previous  $\rho_c$  studies on p<sup>+</sup>-Ge (Fig. 8) used junctions deeper than 100 nm [3]–[9], but as discussed in this work, the shallow junction creates extra difficulty in achieving both low  $R_{sh}$  and low  $\rho_c$ . Hence further investigations are still required to improve both the contact and the shallow junction performance for the downscaled p-Ge transistors.

#### V. CONCLUSIONS

NiGe/p<sup>+</sup> Ge contacts show low thermal stability that cannot survive the thermal budget in standard manufacturing. In contrast, Ti/p<sup>+</sup>Ge contacts show adequate stability, provide low contact resistance, and are thus a better candidate

for the p-Ge devices. In addition, we demonstrate the advantageous multi-pulse laser (MPL) for B activation: a  $\rho_c$  of  $1.1 \times 10^{-8} \Omega \cdot \text{cm}^2$  is achieved by Ti contacts on p<sup>+</sup>-Ge substrate activated by MPL.

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